CLAIMS

[1] A semiconductor device comprising:

two level shift switches each having first and second electrodes, a control electrode, a signal output electrode, and a first semiconductor region forming a transistor device section which intervenes between said first electrode and said signal output electrode and is brought into or out of conduction according to a signal inputted to said control electrode and a resistor device section which intervenes between said signal output electrode and said second electrode, said first semiconductor region comprising a wide bandgap semiconductor; and

a diode having a cathode-side electrode, an anode-side electrode, and a second semiconductor region comprising a wide bandgap semiconductor.

[2] The semiconductor device according to claim 1, wherein: said first semiconductor region of each of said level shift switches has: a wide bandgap semiconductor substrate of a first conductivity type; a drift layer of the first conductivity type formed on said wide bandgap semiconductor substrate; a well region of a second conductivity type formed in a surface region of said drift layer exclusive of a part of the surface region; a source region of the first conductivity type formed in a predetermined region of a surface of said well region; and a RESURF region spaced apart from said source

region and formed to extend over said well region and said part of the surface region of said drift layer, said RESURF region being of the first conductivity type or of a stacked structure comprising a first conductivity type semiconductor and an intrinsic semiconductor;

said first electrode is formed on said source region; said control electrode is formed over a portion of said well region lying intermediate said source region and said RESURF region with a gate insulator intervening therebetween; said signal output electrode is formed on said RESURF region; and said second electrode is formed on a reverse side of said wide bandgap semiconductor substrate; and

said well region, said source region and said RESURF region form said transistor device section; and said RESURF region, said drift layer including said part of the surface region and said wide bandgap semiconductor substrate form said resistor device section.

[3] The semiconductor device according to claim 2, wherein a channel region comprising a wide bandgap semiconductor which is of the first conductivity type or of a stacked structure comprising a first conductivity type semiconductor and an intrinsic semiconductor is formed immediately under said gate insulator to interconnect said source region of the first conductivity type and said RESURF region of the first conductivity type or of said stacked structure comprising a first conductivity type semiconductor

and an intrinsic semiconductor.

[4] The semiconductor device according to any one of claims 1 to 3, wherein said second electrodes of respective of said two level shift switches and said cathode-side electrode of said diode are integrated into a common electrode.

[5] The semiconductor device according to claim 1, wherein said first semiconductor region of each of said two level shift switches and said second semiconductor region of said diode are formed of a same wide bandgap semiconductor substrate and a same wide bandgap semiconductor region formed thereon.

[6] The semiconductor device according to claim 5, wherein: said wide bandgap semiconductor substrate forming said first semiconductor region of each of said level shift switches is of a first conductivity type; said wide bandgap semiconductor region forming said first semiconductor region of each of the level shift switches has: a drift layer of the first conductivity type formed on said wide bandgap semiconductor substrate; a well region of a second conductivity type formed in a surface region of said drift layer exclusive of a part of the surface region; a source region of the first conductivity type formed in a predetermined region of a surface of said well region; and a RESURF region spaced apart from said source region and formed to extend over said well region and said part of the surface region of said drift layer, said RESURF region being of the

first conductivity type or of a stacked structure comprising a first conductivity type semiconductor and an intrinsic semiconductor;

said first electrode is formed on said source region; said control electrode is formed over a portion of said well region lying intermediate said source region and said RESURF region with a gate insulator intervening therebetween; said signal output electrode is formed on said RESURF region; and said second electrode is formed on a reverse side of said wide bandgap semiconductor substrate; and

said well region, said source region and said RESURF region form said transistor device section; and said RESURF region, said drift layer including said part of the surface region and said wide bandgap semiconductor substrate form said resistor device section.

[7] The semiconductor device according to claim 6, wherein a channel region comprising a wide bandgap semiconductor which is of the first conductivity type or of a stacked structure comprising a first conductivity type semiconductor and an intrinsic semiconductor is formed immediately under said gate insulator to interconnect said source region of the first conductivity type and said RESURF region of the first conductivity type or of said stacked structure comprising a first conductivity type semiconductor and an intrinsic semiconductor.

[8] The semiconductor device according to any one of

claims 5 to 7, wherein said second electrodes of respective of said two level shift switches and said cathode-side electrode of said diode are integrated into a common electrode located on a reverse side of said wide bandgap semiconductor substrate, while said first electrode and said signal output electrode of each of said two level shift switches and said anode-side electrode of said diode located on an obverse side of said wide bandgap semiconductor substrate.

[9] The semiconductor device according to any one of claims 5 to 8, wherein said two level shift switches and said diode are each device-isolated by a mesa structure or a p-n junction on the obverse side of said wide bandgap semiconductor substrate.

[10] The semiconductor device according to any one of claims 1 to 9, wherein said diode is a Schottky diode having a Schottky electrode as said anode-side electrode.

[11] The semiconductor device according to any one of claims 1 to 10, wherein said wide bandgap semiconductor is silicon carbide.

[12] A module for use in an inverter device including at least one combination of:

an inverter main circuit section having: a high-side power switching device which has a high potential side electrode connected to a high potential side power supply line and which is ON/OFF-controllable according to a high-side gate drive signal; a low-side power switching device which has a

low potential side electrode connected to a low potential side power supply line and which is ON/OFF-controllable according to a low-side gate drive signal; and an output terminal connected to a low potential side electrode of said high-side power switching device and a high potential side electrode of said low-side power switching device, said high-side power switching device and said low-side power switching device being connected in series between the high potential side power supply line and the low potential side power supply line which are to be applied with d.c. voltage;

a low-side gate drive circuit to be supplied with a source voltage from a low-side gate drive power supply to generate and output a gate drive signal for said low-side power switching device according to a low-side control signal for ON/OFF-controlling said low-side power switching device;

a capacitor having a one-side electrode electrically connected to said output terminal;

a diode having a cathode-side electrode connected to an other-side electrode of said capacitor and an anode-side electrode into which a current from said low-side gate drive power supply flows when said low-side power switching device is turned ON;

a first level shift switch which includes first and second electrodes, a control electrode and a signal output electrode, said first electrode being electrically connected to said low potential side power supply line, said second

electrode being electrically connected to said other-side electrode of said capacitor, and which is configured to perform an operation such that when a first pulse is inputted to said control electrode at start of a period during which said high-side power switching device is to be kept ON, a second pulse having a potential that depends upon a potential of the other-side electrode of said capacitor and is higher than a potential of said first pulse is outputted from said signal output electrode;

a second level shift switch which includes first and second electrodes, a control electrode and a signal output electrode, said first electrode being electrically connected to said low potential side power supply line, said second electrode being electrically connected to said other-side electrode of said capacitor, and which is configured to perform an operation such that when a third pulse is inputted to said control electrode at end of said period during which said high-side power switching device is to be kept ON, a fourth pulse having a potential that depends upon a potential of said other-side electrode of said capacitor and is higher than a potential of said third pulse is outputted from said signal output electrode;

a signal generating circuit to be supplied with a voltage across the opposite ends of said capacitor as a source voltage and configured to generate and output a high-side control signal for turning ON said high-side power switching

device in a manner timed to the output of said second pulse from said signal output electrode of said first level shift switch and turning OFF said high-side power switching device in a manner timed to the output of said fourth pulse from said signal output electrode of said second level shift switch; and

a high-side gate drive circuit to be supplied with a voltage across the opposite ends of said capacitor as a source voltage and configured to generate and output a gate drive signal for said high-side power switching device according to said high-side control signal outputted from said signal generating circuit,

the module comprising at least one combination of: a conductive substrate on which the semiconductor device comprising said first and second level shift switches and said diode according to any one of claims 1 to 11 and said low-side power switching device are mounted, the conductive substrate being electrically connected to said output terminal; said capacitor having said one-side electrode connected to said conductive substrate and said other-side electrode electrically connected to said second electrode of each of said two level shift switches of said semiconductor device and to said cathode-side electrode of said diode; said high-side power switching device having said low potential side electrode electrically connected to said conductive substrate; said signal generating circuit electrically connected to said signal output electrode of each of said two level shift

switches of said semiconductor device and to said capacitor; and said high-side gate drive circuit electrically connected to each of said signal generating circuit, said high-side power switching device and said capacitor.

[13] The module according to claim 12, wherein said capacitor is a chip capacitor mounted on said conductive substrate and said semiconductor device is mounted as stacked on said capacitor.

[14] The module according to claim 13, wherein said conductive substrate on which said low-side power switching device, said chip capacitor and said semiconductor device are mounted is mounted as stacked on said low potential side electrode of said high-side power switching device.

[15] The module according to any one of claims 12 to 14, wherein a chip comprising said signal generating circuit and said high-side gate drive circuit is mounted as stacked on said high-side power switching device.